High-Temperature Applications of SIMOX Technology

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Abstract

High-temperature operation of regular bulk CMOS integrated circuits is usually limited to approximately 200°C because of the increase of the junction leakage currents, the drift of the threshold voltage, the degradation of the mobility in the transistors, and thermally-induced latchup. In addition to these strictly device-related parameter variations, other degradation mechanisms are raising reliability issues when high-temperature operation is to be considered. These are: increased electromigration phenomena in aluminum lines, stress and corrosion in the package, etc... While the latter problems can be solved by using tungsten as an interconnect metal and by using appropriate packaging materials, the drift of device parameters with temperature is a problem having no solution as long as classical bulk silicon MOS technology is employed.

Introduction

Silicon-on-insulator (SOI) technology, and, in particular, SIMOX (Separation by IMplantation of OXygen) technology, is fully compatible with the techniques and the equipments used for standard silicon CMOS processing. In addition to the classical benefits associated with the use of SOI substrates (higher-speed operation, easy processing, ...) [1], SOI MOSFETs presents interesting features as far as high-temperature operation is concerned. Indeed, thin-film SIMOX MOSFETs made in thin-film SIMOX substrates present very small junction areas, and their high-temperature leakage current can be 3 to 4 orders of magnitude lower than those of regular MOS devices. In addition, the threshold voltage variation with temperature is much smaller in thin-film SIMOX MOSFETs than in bulk devices. Functionality of 16k and 256k SRAMs at high temperatures (up to 300 °C) and of SOI CMOS ring oscillators up to 500°C has been demonstrated in the past [2-4]. This paper reviews the basic properties of thin-film SIMOX MOS devices and circuits used for high-temperature operation.

SOI MOSFET parameters

There exists different types of SOI MOSFETs. If the devices are made in relatively thick silicon films (> 200 nm), there exists a portion of neutral silicon beneath the depletion zone in the channel region. Such devices are called "partially depleted transistors". If the silicon film is thinner than the maximum vertical extension of the space-charge region (≤ 100 nm, typically), the entire silicon film can be depleted of majority carriers in the channel region. Such devices are called "fully depleted transistors".[1] Thin-film accumulation-mode transistors can be realised as well. In these devices, the silicon film beneath the channel is doped P-type in p-channel devices, and N-type in n-channel devices. In the OFF state, the channel region is fully depleted of majority carriers, while a surface accumulation channel is formed in the ON state.[1] It is also possible to fabricate transistors where the gate electrode covers both the top and the bottom of the active silicon film. An example of such a device is the "Gate-All-Around" (GAA) MOSFET.[1]

Some device parameters, such as the channel mobility, vary with temperature in SOI devices like in bulk MOSFETs. Some other parameters, on the other hand, vary in quite a different way. The most important of these parameters are the junction leakage current, the threshold voltage and, as far as analog applications are concerned, the output conductance.

Leakage current

Classical PN junction theory tells us that the leakage current of a reverse-biased diode contains two components: a diffusion current, the amplitude of which is proportional to the square of the intrinsic carrier concentration ($I_{diff} \propto n_i^2(T)$), and a generation current, which shows a linear dependence upon the intrinsic carrier concentration ($I_{gen} \propto n_i(T)$). In bulk silicon junctions at room temperature the generation current is usually larger than the diffusion current, but this situation gets reversed at high temperatures because of the stronger temperature dependence of the diffusion current [7]. In thin-film SIMOX devices it has been observed that the junction leakage current is proportional to $n_i(T)$ if the body of the device is fully depleted when the transistor is turned off. This is always the case in accumulation-mode SOI MOSFETs (Figure 1). This is also the case in enhancement-mode, fully depleted devices up to a critical temperature where the increase of the intrinsic carrier concentration is such that the device

is no longer fully depleted. Only above that critical temperature an $n_i^2(T)$ dependence of the leakage current on temperature is observed.

The device OFF current, which is equal to the reverse-biased drain junction in enhancement-mode SOI MOSFETs, is markedly smaller in SOI than in bulk transistors, owing, on one hand, to the reduced junction area and, on the other hand, to the $n_i(T)$ increase of the current with temperature [5]. This observation is also valid for accumulation-mode devices. Figure 2 presents the drain current as a function of gate voltage in accumulation-mode p-channel SOI devices, where I_{ON}/I_{OFF} ratios in excess of 10,000 and 100 are obtained at 200 and 300°C, respectively. Owing to these high I_{ON}/I_{OFF} ratios SIMOX logic circuits are still functional at high temperatures.

In addition to the fact that the area of source and drain junctions is much smaller in SOI than in bulk (by a factor of 15 to 100 depending on the design rules), it is also worthwhile noting that the largest of all junctions, the well junctions, are totally absent from SOI CMOS. This contributes to a drastic reduction of the overall standby current consumption of SOI circuits, compared to bulk CMOS. Figure 3 presents the junction leakage paths in bulk and SOI CMOS inverters. In the bulk device leakage currents flow to the substrate from the reverse-biased well junction and from the reverse-biased drain of the n-channel MOSFET (the case where the output is "high" is considered here). In the SOI inverter the only leakage current to be considered is the n-channel drain junction leakage. Consequently, the high-temperature standby power consumption is much smaller in the SOI inverter than in the bulk device.

SOI compares even more favourably to bulk when more complex devices, such as logic gates, are considered. Figure 4 presents a NAND gate having both a high and a low input bias. In the bulk device there are three reverse-biased sources or drains in addition to the reverse-biased well. The leakage currents of all these junctions flow simultaneously (in parallel) towards the substrate, such that the overall standby current consumption of the gate is given by the sum of all leakage currents. In the SOI gate, on the other hand, no current is allowed to flow towards the substrate, which is dielectrically isolated from the devices. The only leakage path from supply to ground is along the branches of the circuit. If several devices are placed in series (which is the case for the n-channel transistors in our NAND gate), the overall standby current is limited to the internal leakage of the least leaky transistor of the series association. It has been observed, for example, that the static power consumption of a SIMOX CMOS NAND gate increases from 0.1 to 5 microamperes when the temperature is raised from 20 to 320°C, which corresponds to a mere 50-fold increase of current consumption. The obvious result of these observations is the following. Functionality of bulk CMOS integrated circuits is affected by high standby current consumption starting from ...150°C..., and these circuits cease to function at a temperature of approximately 200°C [2] due to excessive current flow in the junctions. SOI circuits, on the other hand, continue to function properly above 300°C without noticeable degradation due to excess leakage currents.

Threshold voltage

The threshold voltage of SOI fully-depleted transistors is known to be 2 to 3 times less sensitive on temperature than that of bulk devices [6]. When the temperature is raised, the intrinsic carrier concentration increases and the Fermi potential decreases. As a result, the work function difference between the polysilicon gate and the active silicon, Φ_{MS}, gets modified and the maximum depletion width in the silicon, X_{dmax}, decreases. In bulk devices, the temperature dependence of both of Φ_{MS} and X_{dmax} contributes to a decrease of the threshold voltage as temperature is increased. In enhancement-mode fully-depleted and accumulation-mode SOI devices, there is no variation of X_{dmax} with temperature. There exists a critical temperature (220°C in [6]), however, beyond which the devices are

no longer fully depleted, which causes the threshold voltage variation with temperature to be similar to that in a bulk device. In some SOI devices, such as transistors with top and bottom gates [5], where depletion arises from both the top and the bottom of the silicon film, this critical temperature is increased substantially, such that minimal temperature dependence of the threshold on temperature is observed up to 320°C (Figure 5).

Output conductance

The output conductance of transistors is an important parameter limiting the performances of analog CMOS ICs. Because the body of the devices is electrically floating, impact ionization-related effects (kink effect, parasitic bipolar action,...)[1] tend to degrade the output conductance of SOI MOSFETs. This degradation is minimized, but nevertheless present, if fully depleted devices are used. It is observed that the output conductance of SIMOX MOSFETs actually improves when temperature is increased [5], as can be seen in Figure 6. This is explained by several mechanisms: high temperature reduces impact ionization near the drain, excess minority carrier concentration in the device body is reduced through increased recombination, and the body potential variations are reduced owing to an increase of the saturation current of the source junction.

Performances of SIMOX circuits at high temperatures

As mentioned earlier, the excellent behaviour of thin-film SIMOX MOSFETs at high temperature makes SIMOX technology highly suitable for high-temperature IC applications. Indeed, the major causes of failure in bulk CMOS logic at high temperature, *i.e.* excess power consumption and degradation of logic levels and noise margin, are observed to be much reduced in SOI circuits. Latch-up is of course totally suppressed when SIMOX technology is used. SIMOX CMOS inverters exhibit full functionality and very little change in static characteristics at temperatures up to 320°C.[5] The switching voltage remains stable, owing to the remarkably weak and symmetrical variation of the n- and p-channel threshold voltages. The output voltage swing is reduced from only a few millivolts at 320°C, due to the slightly increased leakage current of the OFF devices and the reduced carrier mobility of the ON devices. This degradation is, however, totally negligible when compared to what is observed in bulk devices. In logic gates with series transistors, such as AND and NAND gates, the increase of standby supply current with temperature remains even more limited than expected on basis of the leakage current of all constituent devices (Figure 4). This is because in SOI circuits, the drain leakage current of each individual transistor flows towards its source, and thus into the following transistor, unlike in bulk circuits, where all drain leakage currents are collected by the substrate.

The best way to assess the influence of temperature on the performances SOI CMOS circuits is to study the behaviour of simple basic circuits. For example, circuit speed has been tested on toggle-chain frequency dividers (divide-by-32). Bulk dividers implemented in static CMOS logic start to behave erratically around 180°C and fail to function at about 225°C. A similar implementation of the dividers in SIMOX technology is still functional at 320°C (Figure 7). The maximum frequency of operation at 320°C is half that achieved at room temperature [5], due to the reduction of carrier mobility.

In a similar way, the holding time characteristics of dynamic gates (clocked NOR gates) have been showed to degrade by a factor 10 only at 320°C, compared to room temperature [5]. This excellent result is, of course, due to the limited increase of the leakage current in SOI devices. As mentioned earlier, functionality of larger circuits, such as 16k and 256k SRAMs at high temperatures (up to 300 °C) has been demonstrated as well [2,3].

The performances of analog circuits depend on other device parameters than digital circuits. For instance, standby current consumption is fixed by the operating point of the circuit rather than by junction leakage. One important parameter is the output conductance of the transistors. Indeed, the dc voltage gain of an operational amplifier (Operational Transconductance Amplifier, OTA) is proportional to the product of the transconductance of the input transistors by the output impedance of the output transistors. As the temperature is increased, the transconductance of the input transistor decreases because of the reduction of carrier mobility with temperature. The output impedance (the inverse of the output conductance), on the other hand, increases as temperature is increased (Figure 6). Owing to this kind of compensation effect in the input transconductance-output impedance product, the resulting dc gain of the overall amplifier is expected to be relatively independent of temperature. The measured characteristics of the device are consistent with what can be expected from theory: as the gate transconductance decreases and the output impedance increases, the dc gain of the SIMOX CMOS amplifier remains quite stable, as presented in Figure 8. It is also worth noting that the offset voltage of the amplifier remains between 0 and 2 millivolts for all temperatures between 20 to 300°C [5]. Such amplifiers are suitable for A-to-D converters and switched capacitor circuits having to operate in a high-temperature environment.

Applications

The excellent behaviour of both analog and digital SOI (SIMOX) CMOS circuits at high temperatures suggests the use of this technology for different applications. Classical industrial applications such as well logging can take advantage of SOI CMOS for *in-situ* signal amplification and data processing in the high-temperature environment encountered deep inside earth's crust. The temperature ranges within which electronic devices may have to work in oil wells, gas wells, steam injection processes and geothermal energy plant applications are listed in Table 1.

Automotive industry and aerospace are also big potential consumers of SOI CMOS. Indeed, car electronics (engine and bake control systems, as well as underhood electronics) has a growing need for both analog and digital circuits which are able to withstand temperatures of 200°C or above. Underhood electronics must be able to withstand relatively high temperatures when a car is parked in the hot sun (up to 200°C). Much higher temperature tolerance is asked from engine monitoring electronics, such electronic injection systems, where precision control of the injector position is controlled by electronic components located close or within the engine block. Modern antilock breaking systems (ABS) also require electronic control systems placed close to the brakes and, therefore, submitted to high temperatures when the brakes are activated. The ability of SOI CMOS to operate at high-temperatures, combined with the possibility of integrating power devices with low-power logic on a single, dielectrically isolated substrate, renders SIMOX the ideal technology for such purposes [9,10]. High-temperature airplane applications include on-board electronics and, of course, engine control and surface control (wing temperature, ...). Space applications are also concerned. Indeed, thermal shielding for satellites is quite heavy, and the weight of a satellite has a direct impact on how much it costs to place it on orbit. In some special applications (Venus probes), shielding is no longer possible and high-temperature electronics is absolutely required. Commercial nuclear applications (power plants,...) also require high-temperature electronics for core control. Table 1 contains a non-exhaustive list of the temperature requirements for high-temperature electronics applications. SIMOX technology can be used for a variety of these applications.

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Table and Figure captions

Figure 1: Off leakage current dependence on temperature of SIMOX (W/L=20μm/5μm) accumulation-mode pMOS transistors for zero back gate and -3 V drain biases, and of a pMOS bulk transistor (W/L=20μm/5μm) with -3 V drain and zero substrate and well biases. Evolutions proportional to n_i and n_i^2 are also indicated (dashed lines). The gate oxide, film and buried oxide thicknesses are equal to 55, 100 and 400 nm respectively in the SIMOX device. The gate oxide of the bulk device is 5 nm thick.

Figure 2: Logarithmic curves of the drain current as a function of the gate voltage in p-channel SIMOX transistors, for different temperatures. The gate oxide, film and buried oxide thicknesses are equal to 55, 100 and 400 nm respectively. W/L=20μm/5μm.

Figure 3: Leakage current paths in bulk (top) and SIMOX (bottom) CMOS inverters. No current flow to the substrate is allowed in SIMOX.

Figure 4: Leakage current paths in a bulk (left) and an SIMOX (right) CMOS NAND gate. Both gates have a high and a low input bias. All bulk junction leakage currents flow in parallel towards the substrate. The leakage of the SIMOX gate is limited to that of a single transistor.

Figure 5: Variation of the threshold voltage in thin-film SIMOX GAA MOSFETs (n- and p-channel) with temperature [5].

Figure 6: Variation of the output conductance in thin-film SIMOX MOSFETs (n- and p-channel) with temperature. W/L=20μm/10μm and V_{GS}=±1.5 V.

Figure 7: Measured input (100 MHz) and output (3.125 MHz) signals of a SIMOX CMOS divide-by-32 circuit operating at 300°C.

Figure 8: Low-frequency gain of a SIMOX operational amplifier *vs.* temperature.

Table 1: Temperature requirements for electronics components used in several consumer or industrial applications.

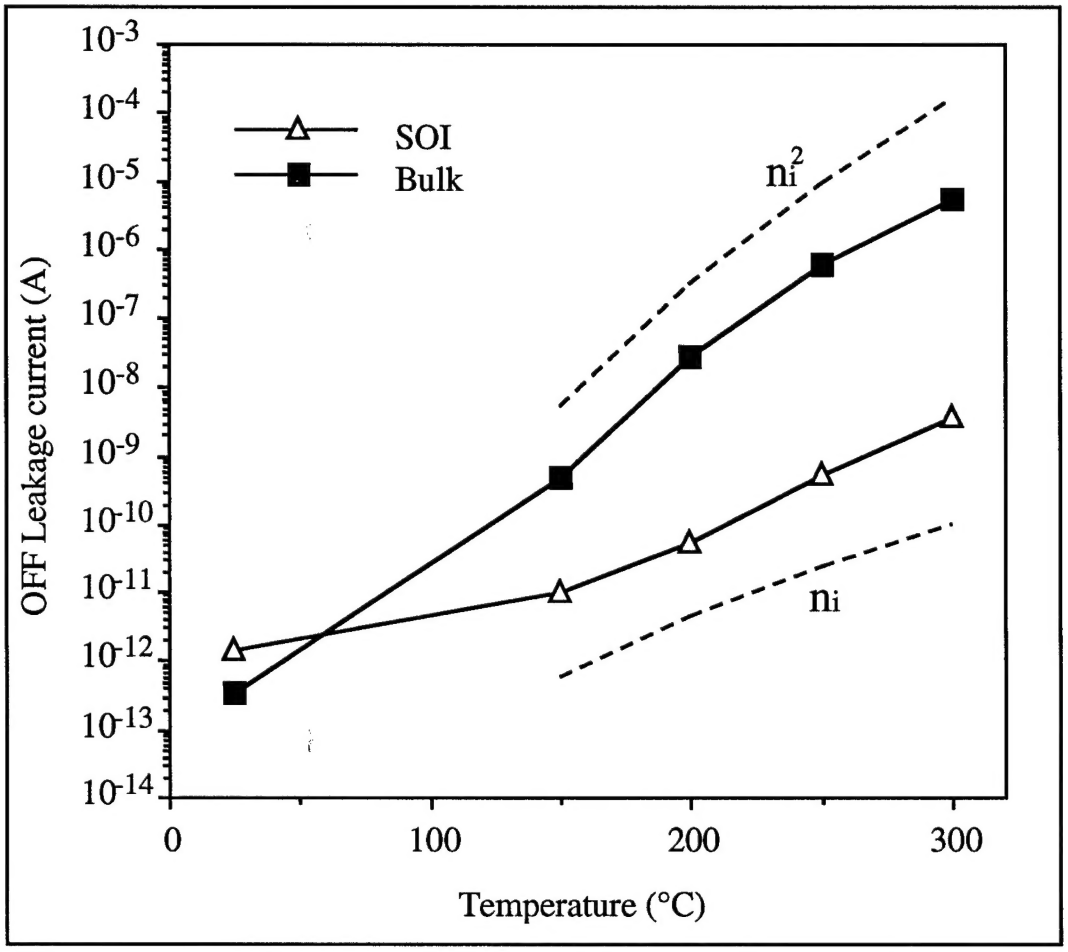
OFF Leakage current (A)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
SOI
Bulk
ni2
ni
0
100
200
300
Temperature (°C)

Figure 1

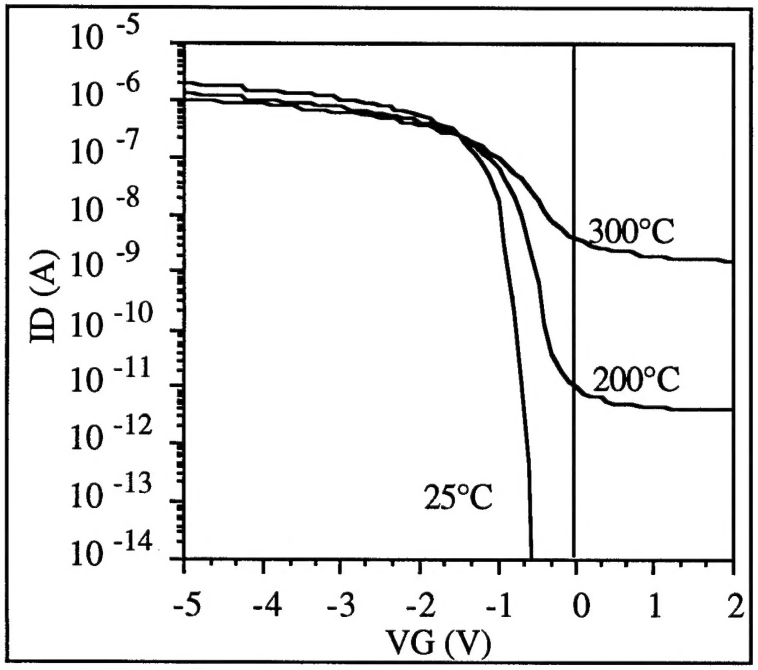
10 -5
10 -6
10 -7
10 -8
10 -9
10 -10
10 -11
10 -12
10 -13
10 -14
ID (A)
300°C
200°C
25°C
-5 -4 -3 -2 -1 0 1 2
VG (V)

Figure 2

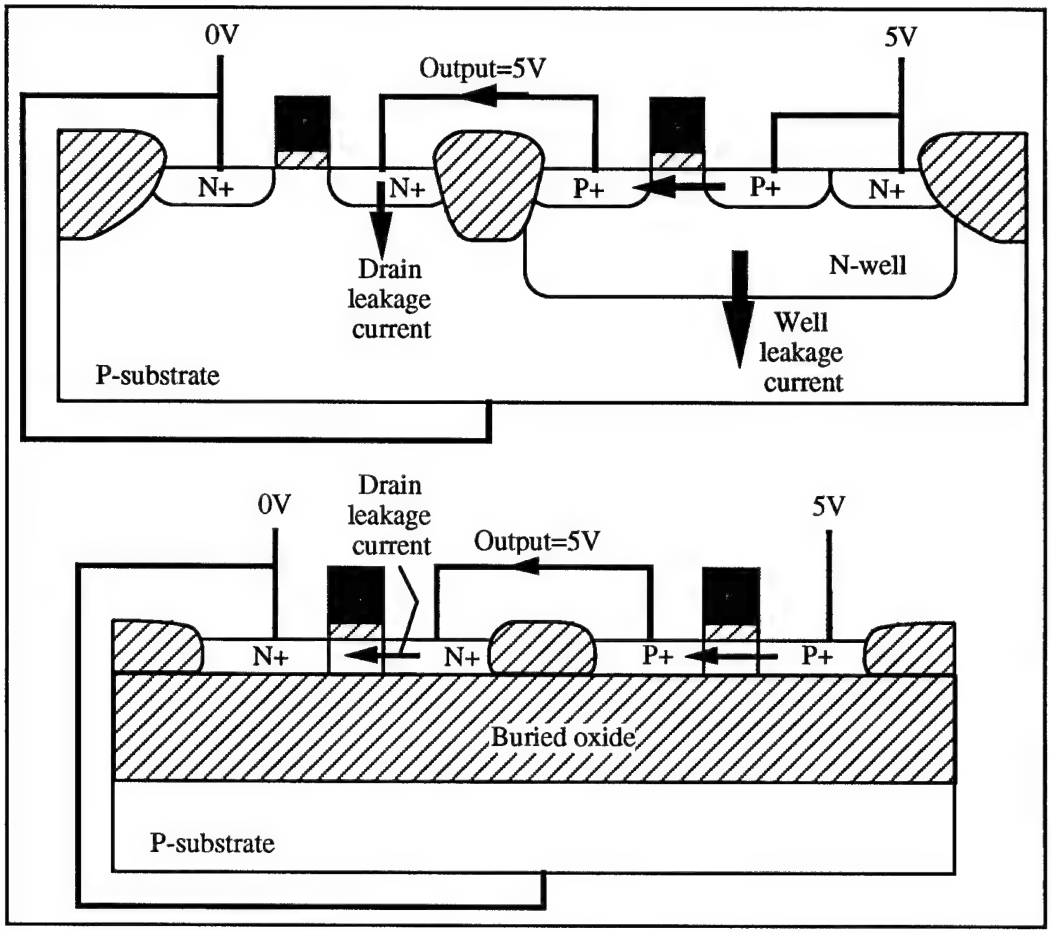
0V
Output=5V
5V
N+
N+
P+
P+
N+
Drain
leakage
current
N-well
Well
leakage
current
P-substrate
0V
Drain
leakage
current
Output=5V
5V
N+
N+
P+
P+
Buried oxide
P-substrate

Figure 3

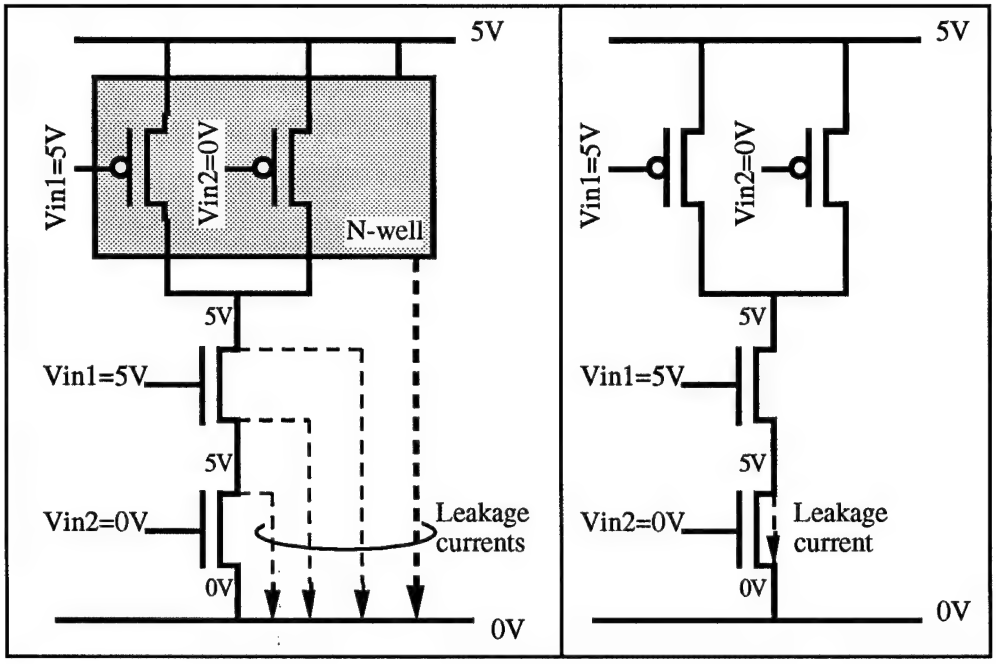
5V
Vin1=5V
Vin2=0V
N-well
5V
Vin1=5V
5V
Vin2=0V
Leakage
currents
0V
0V
5V
Vin1=5V
Vin2=0V
5V
Vin1=5V
5V
Vin2=0V
Leakage
current
0V
0V

Figure 4

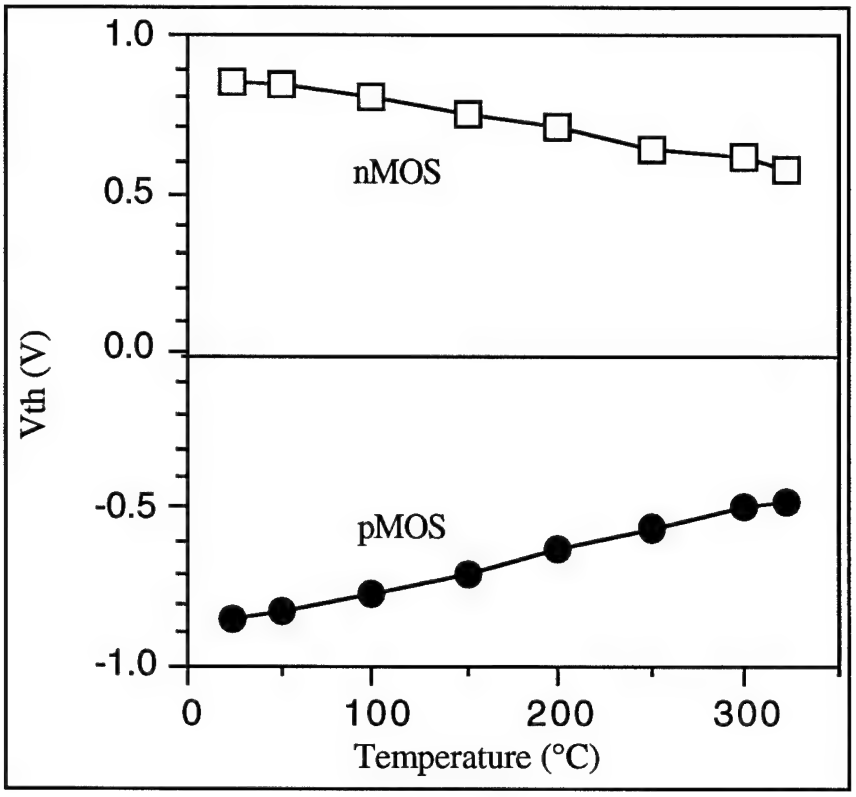

Figure 5

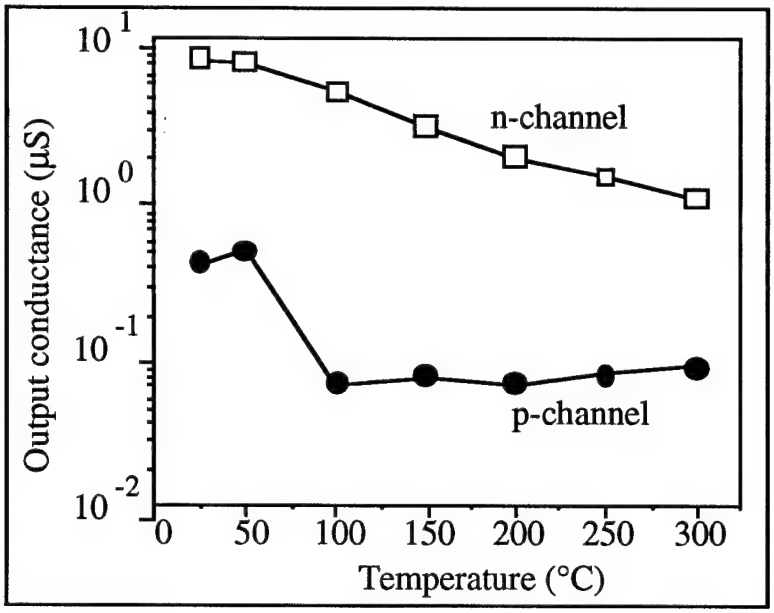
Output conductance (μS)
10 1
10 0
10 -1
10 -2
n-channel
p-channel
0
50
100
150
200
250
300
Temperature (°C)

Figure 6

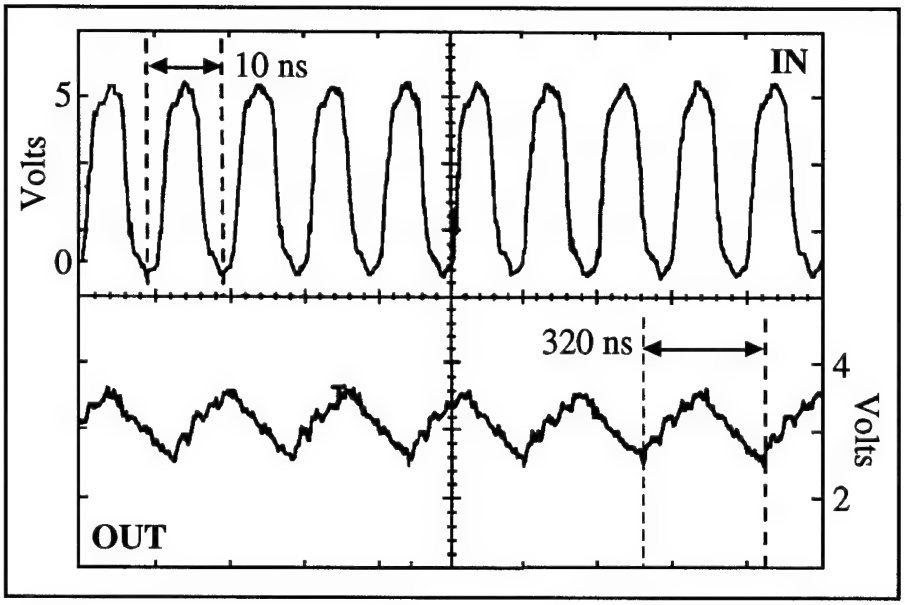

Figure 7

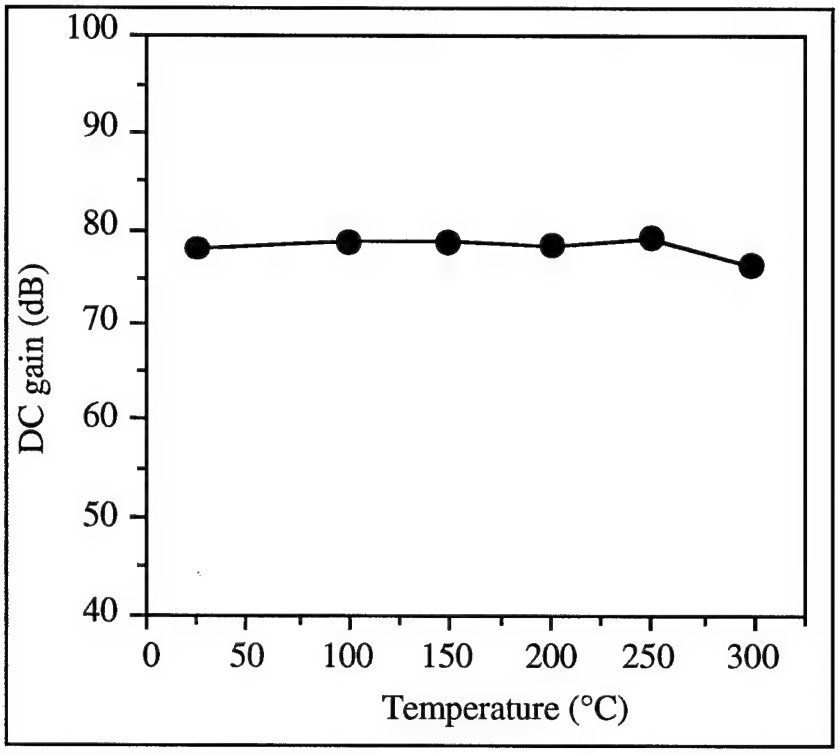
100
90
80
70
60
50
40
DC gain (dB)
0
50
100
150
200
250
300
Temperature (°C)

Figure 8

Application	Temperatures
Well logging	75-600°C
Oil wells	75-175°C
Gas wells	150-225°C
Steam injection	200-300°C
Geothermal energy	200-600°C
Automotive	150-600°C
Underhood	-50-200°C
Engine sensors	up to 600°C
Combustion & exhaust sensors	up to 600°C
ABS	up to 300°C
Aircraft	150-600°C
Internal equipment	150-250°C
Engine monitoring	300-600°C
Surface controls	300-600°C
Satellites (Venus probe)	150-600°C
Commercial nuclear	30-550°C

Table 1

Demonstration of the Potential of Accumulation-Mode MOS Transistors on SOI Substrates for High-Temperature Operation (150–300°C)

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Abstract—**Measurements of accumulation-mode (AM) MOS SOI transistors in the 150–300°C temperature range are reported and discussed. The increases of the threshold voltage shift and off leakage current with temperature of these SOI p-MOSFET's are observed to be much smaller than their bulk equivalents. Simple models are presented to support the experimental data.**

I. Introduction

APPLICATIONS in the areas of engine control, well logging, nuclear power plants, etc. have created a demand for integrated circuits functioning at high temperatures (~ 300°C) [1]. Conventional bulk CMOS circuits usually fail in this temperature range due to threshold voltage shifts, excessive junction leakage currents, thermal latch-up activation, etc. The benefits of enhancement-mode fully depleted MOS SOI transistors for high-temperature operation have already been demonstrated, and 2 to 3 times smaller threshold voltage shifts [2] and 3 to 4 orders of magnitude smaller leakage currents [3] have been reported. More recently, accumulation-mode MOS SOI transistors have emerged as promising devices for high-performance CMOS applications [4]. Much attention has been paid to the physics at room temperature of these unique devices, characterized by source, drain, and body regions of the same doping polarity and featuring three distinct conduction mechanisms in the film, namely accumulation at the front and back interfaces and body current in a central neutral region [5], [6]. In the present paper, experimental results demonstrating the potential and capability of accumulation-mode p-MOS SOI transistors for high-temperature applications are presented and discussed for the first time.

II. Experiment

We have used two types of accumulation-mode (AM) p-MOS transistors realized on SIMOX substrates. In the first case (SOI1), gate oxide, film, and buried oxide thicknesses were 15, 90, and 400 nm, and in the other (SOI2) they were 55, 100 and 400 nm, respectively. The p-type body doping level was about 4×10^{16} cm^{-3} for type 1 and 10^{16} cm^{-3} for type 2. The gate material was n$^+$-poly in both cases. Measurements of drain current versus gate voltage characteristics (I_d–V_g) were performed on a temperature-regulated hot chuck at different drain and back-gate biases in the range 25–300°C. The maximum temperature corresponds to the limit of our measurement setup, not to device breakdown. Similar experiments were also carried out for sake of comparison, on p-MOS bulk transistors featuring a gate oxide thickness of 55 nm and an n-type doping level of about 10^{16} cm^{-3}. The n-well was fixed at the substrate potential in order to suppress the well leakage current and focus on the intrinsic device characteristics, which is a favorable condition for the bulk case. The benefits of the SOI devices with respect to the threshold voltage (V_{th}) and off leakage current (I_{off}) dependences on the temperature (T) are clearly evidenced by Fig. 1. We will now discuss in more details these two subjects of interest.

A. Threshold Voltage

V_{th} was extracted from I_d–V_g curves at low drain bias (−50 mV) for the different devices (Fig. 2). The AM p-MOS SOI transistors exhibit a remarkably low V_{th} shift with T ranging from 1.3 to 1.55 mV/°C compared to the 2.7 to 3.3 mV/°C in conventional bulk devices. A physical explanation for that significant difference may be derived from simple $\partial V_{th}/\partial T$ models. In the case of a bulk MOSFET, one obtains, assuming for simplification that the Si bandgap and oxide charge density are independent of temperature [2]:

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial \Phi_F}{\partial T}\left[1 + q\frac{t_{ox}}{\epsilon_{ox}}\sqrt{\frac{\epsilon_{si}N}{kT\ln(N/n_i)}}\right] \quad (1)$$

where Φ_F is the Fermi potential, q is the electron charge, t_{ox} is the gate oxide thickness, N is the doping level, k is Boltzmann's constant, n_i is the Si intrinsic carrier concentration, and ϵ_{si} and ϵ_{ox} are the Si and oxide permittivities. The square-root term in (1) is related to the temperature dependence of the maximum depletion width at the

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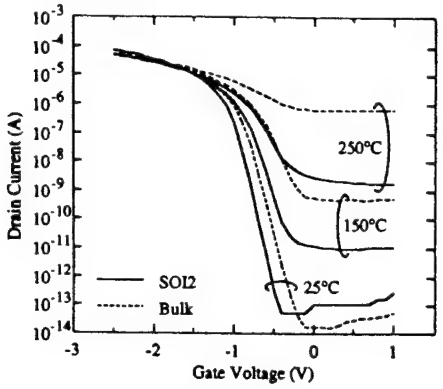

Fig. 1. Drain current versus gate voltage characteristics of 20-μm-wide, 5-μm-long SOI and bulk devices at different temperatures, for a −3-V drain bias: accumulation-mode p-MOS SOI transistor of type SOI2 with a zero back-gate bias, and p-MOS bulk transistor with zero substrate and well biases.

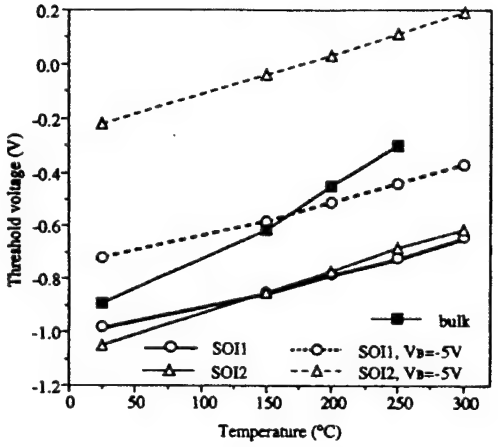

Fig. 2. Threshold voltage variation with temperature of accumulation-mode p-MOS SOI transistors for back-gate biases, V_B, of 0 and −5 V and of a p-MOS bulk device for zero substrate and well biases.

inversion threshold. In the case of AM MOS SOI devices, using identical approximations, we derive from our V_{th} model at room temperature [7]:

$$\frac{\partial V_{th}}{\partial T} = [1 + \alpha]\frac{\partial \Phi_F}{\partial T} \tag{2}$$

where in the normal domain of operation, α ranges from $(\epsilon_{si}t_{ox})/(\epsilon_{ox}t_{si} + \epsilon_{si}t_{ob})$ to $(\epsilon_{ox}t_{si} + \epsilon_{si}t_{ox})/(\epsilon_{si}t_{ob})$ depending on the back-gate bias, t_{si} being the film thickness and t_{ob} the buried oxide thickness. The new α term is related to the unique threshold condition in AM SOI devices, i.e., the change from full to partial depletion in the film. Introducing our process parameters and the dependence of n_i on T in (1) and (2), theoretical $\partial V_{th}/\partial T$ values of 1.1 to 1.3 mV/°C were calculated for our SOI devices (depending on α) and 2.4 to 2.8 mV/°C for the bulk (depending on T). These are about 20% below the experimental results, presumably due to the temperature-dependent terms omitted in our crude models. However, the factor of 2 measured between the bulk and SOI devices is correctly predicted, as well as in the SOI case, the dependence of $\partial V_{th}/\partial T$ on t_{ox} and its independence on T, and in the bulk case, the increase of $\partial V_{th}/\partial T$ with T.

Expression (2) may also be useful to compare AM and enhancement-mode (EM) fully depleted (FD) MOS SOI transistors. P-devices of the latter kind feature an n-doped body and operate with surface inversion and full depletion in the film. In this case, figures below 1 mV/°C were reported for devices with similar process parameters and a very simple model was proposed [2]:

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial \Phi_F}{\partial T}. \tag{3}$$

This dependence is obviously smaller than (2) and has been related to the absence, in EM FD devices, of the temperature-induced variation of the depletion depth at inversion threshold, this depth being equal to the film thickness. However, AM transistors retain a considerable advantage over EM FD devices at very high temperatures. Above a critical temperature of about 220°C, EM FD devices reach inversion with partial instead of full depletion of the film. In that case, $\partial V_{th}/\partial T$ increases to values similar to bulk. Our results demonstrate that AM p-MOS SOI transistors do not present such an increase of $\partial V_{th}/\partial T$ up to 300°C, because full depletion can still be maintained in these devices, owing to their reduced film doping level.

B. Off Leakage Current

The amplitude of I_{off} for the different devices under consideration were extracted from I_d–V_g measurements with high drain bias, at a gate voltage of 1 V below V_{th} (Fig. 3). At high temperature, the I_{off} of AM p-MOS SOI transistors is 2 to 3 orders of magnitude smaller than in comparable bulk devices. At 300°C and −3-V drain bias, the I_{off} of our AM devices is a low 1.25 nA/μm of channel width. These results are explained, on one hand, by the total suppression of the drain junction bottom region and the significant reduction of the drain sidewall junction area in SOI devices and, on the other hand, by the I_{off} dependence on T.

In bulk devices, I_{off} mostly corresponds to the reverse current of the p-n drain junction, whose predominant component at high temperature is a diffusion current in neutral regions. The increase of I_{off} with T is hence proportional to $n_i^2(T)$ as observed in our measurements (Fig. 3). In AM MOS SOI devices, we observe that the increase of I_{off} with T is proportional to n_i. This means that I_{off} is mainly related to a generation current in a depletion region. This result could be expected from the theoretical knowledge that in the off regime, the film of AM MOS SOI devices is fully depleted, which removes neutral regions and hence the diffusion component.

In the case of EM FD MOS SOI transistors, I_{off} of 3 to 4 orders of magnitude smaller than in bulk have been

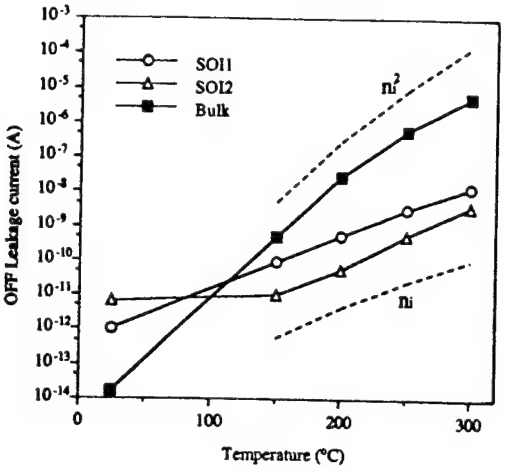

Fig. 3. Off-leakage-current dependence on temperature of SOI1 devices ($W/L = 20\ \mu m/5\ \mu m$) and SOI2 ($W/L = 3\ \mu m/3\ \mu m$) accumulation-mode p-MOS SOI transistors for zero back gate and −3-V drain biases and of a p-MOS bulk transistor ($W/L = 20\ \mu m/5\ \mu m$) with −3-V drain and zero substrate and well biases. Evolutions proportional to n_i and n_i^2 are also indicated (dashed lines).

reported [3]. However, above the critical temperature already mentioned, the n_i evolution of I_{off} with T transforms into an n_i^2 variation, as a result of the appearance of a neutral region in the film. Our measurements anew demonstrate that this behavior is absent from AM p-MOS SOI transistors up to 300°C (Fig. 3), owing to their reduced doping level.

III. Conclusion

The potential of accumulation-mode p-MOS SOI transistors for high-temperature operation, compatible with circuit requirements, has been experimentally demonstrated and theoretically explained in the range of 150–300°C. It has also been shown that these devices are far superior to conventional bulk. They are also superior to enhancement-mode fully depleted MOS SOI transistors at very high temperatures, in terms of full depletion operation.

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High-Temperature Gate Capacitances of Thin-Film SOI MOSFETs

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Abstract

This paper presents original measurements and two-dimensional simulations of high-temperature SOI MOSFET intrinsic gate capacitances. Results regarding threshold voltage extraction, impact ionization effects and subthreshold capacitance are discussed.

1. INTRODUCTION

Thin-film SOI CMOS technology is now considered as a likely candidate for integrated circuit applications at temperatures up to 400°C. Although the operation of digital and analog SOI CMOS circuits has recently been demonstrated at 320°C [1], detailed device characterizations in this temperature range have so far been limited to static current measurements [2, 3]. In the present abstract, measurements and two-dimensional simulations of high-temperature SOI MOSFETs small-signal characteristics are reported, focusing on the intrinsic gate capacitances. To our knowledge, neither SOI nor bulk MOSFET gate capacitance characteristics at high temperature have been discussed before.

2. EXPERIMENTAL RESULTS

Figures 1 and 2 present gate-to-source capacitance (C_{gs}) measurements performed on enhancement-mode n-channel and accumulation-mode p-channel MOS transistors on SIMOX substrates, for various temperatures in the 20-300°C range. Long channel devices (20 µm) were considered in order to avoid disturbing short-channel effects in a primary study. The gate oxide, film and buried oxide are respectively 55, 100 and 420 nm-thick. Several phenomena are clearly dependent on the temperature (T) and will be discussed in the following, mainly: the threshold voltage (V_{th}), an anomalous hump in the nMOSFET capacitance characteristics and the subthreshold capacitance value (C_{off}).

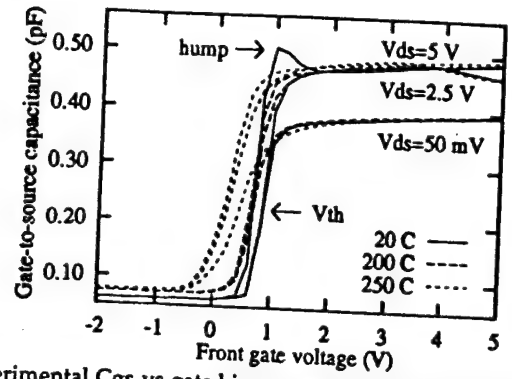

Fig. 1: Experimental Cgs vs gate bias curves of a 50 µm-wide, 20 µm-long SOI n-MOSFET for various drain biases and temperatures (back substrate = 0 V).

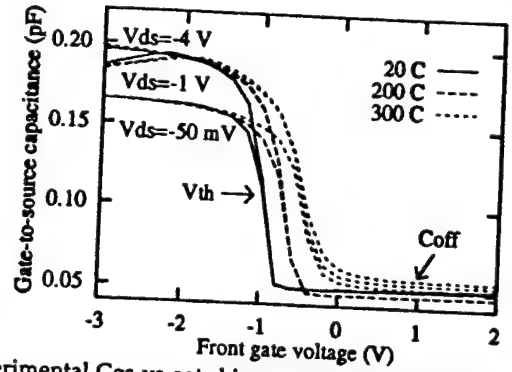

Fig. 2: Experimental Cgs vs gate bias curves of a 20 µm-wide, 20 µm-long SOI p-MOSFET for various drain biases and temperatures (back substrate = 0 V).

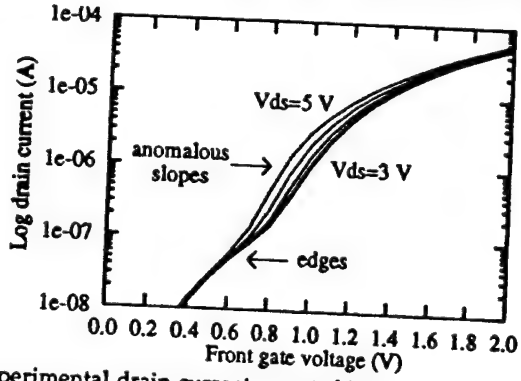

Fig. 3: Experimental drain current vs gate bias curves of a 50 µm-wide, 20 µm-long SOI n-MOSFET for various drain biases at 20°C (back substrate = 0 V).

2.1. Threshold Voltage

The V_{th} variation with temperature in figures 1 and 2 is in fair accordance with values obtained from I-V curves for similar devices [1], i.e. about 1.5 mV/°C, which is much lower than in bulk MOSFETs. Extraction of V_{th} from C_{gs} curves yields a clear advantage over I-V techniques regarding the high sensitivity of the latter to mobility variation and to leakage currents due to either lateral edges (fig. 3) or high temperature operation.

2.2. Impact Ionization Effects

Comparing room temperature C_{gs} and I-V characteristics (figs. 1 and 3), the anomalous C_{gs} hump clearly corresponds to well-known anomalous subthreshold slopes due to impact ionization effects. This also explains the reduction of the hump at higher temperatures.

2.3. Subthreshold Capacitance

At high temperatures, we observe a clear increase of C_{off} over the classical source-gate overlap value. In figure 2, a dependence of C_{off} on the drain voltage is also observed. In figure 1, this dependence only occurs around threshold.

3. DISCUSSION

From MEDICI simulations using a dedicated transient computation scheme [4], these unique phenomena have been correlated with the presence in the SOI film of large numbers of carriers in excess of the normal value. In the case of the C_{gs} hump, these excess charges are created by impact ionization [5].

At high temperature, the carrier concentrations also exceed by far their room temperature value. This gives rise to subthreshold leakage currents as well as to the increase of C_{off} and its dependence on the drain voltage. Figure 4 directly correlates C_{off} with the leakage current. Simulations also show that above 350°C, C_{off} may already amount to a significant part of the total oxide capacitance, although the leakage current is still 2 to 3 orders of magnitude below the ON current (fig. 5, b and c).

To explain the mechanisms leading to these phenomena, we simultaneously plot the simulated C_{gs} and the surface concentration of the carriers connected to source and drain (fig. 5). This demonstrates that C_{gs} abruptly increases when the related carrier concentration exceeds $10^{13}...10^{14}$ cm^{-3}. At room temperature, this occurs at the transition from moderate to strong inversion depending on the gate bias. At high temperature, it may already occur in the subthreshold regime.

4. CONCLUSION

The intrinsic gate capacitance characteristics of SOI MOSFETs have been investigated up to 400°C by experiment and simulations. Differences with room

temperature behaviour have been observed and explained in terms of thermally generated excess carrier concentrations. We believe that similar phenomena also occur in bulk MOSFETs for which intrinsic capacitance measurements are impeded by excessive junction leakage currents.

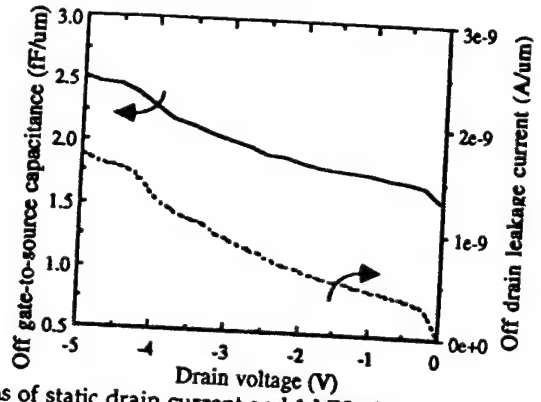

Fig. 4: Simulations of static drain current and 1 MHz Cgs vs drain bias, in the cut-off regime at 300°C, on a 5 µm-long, 1 µm-wide accumulation-mode SOI p-MOSFET.

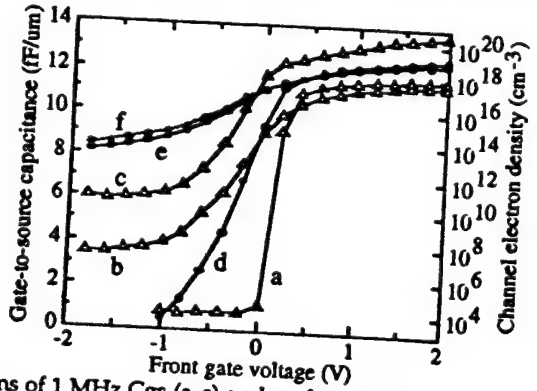

Fig. 5: Simulations of 1 MHz Cgs (a-c) and surface electron density (d-f) vs gate bias, in a 10 µm-long, 1 µm-wide enhancement-mode SOI n-MOSFET, at 25°C (a,d) and 375°C (b,c,e,f) with drain bias equal to 50 mV (a,b,d,e) or 5 V (c,f).

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SOI TECHNOLOGY FOR HIGH-TEMPERATURE APPLICATIONS

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Abstract

This work investigates and demonstrates the potential of Silicon-On-Insulator (SOI) MOSFETs for high-temperature analog and digital applications. The small area of junctions in SOI/MOS devices reduces the high-temperature leakage currents by as much as 3 to 4 orders of magnitude over regular (bulk) MOS devices. The threshold voltage variation with temperature is 2 to 3 times smaller than in bulk devices, and the output conductance of SOI MOSFETs actually improves as temperature is increased. These properties enable the fabrication of digital and analog SOI/CMOS circuits operating up to over 300°C with little performance degradation. This paper describes the high-temperature performances of small SOI/CMOS circuit blocks such as static and dynamic logic gates, frequency dividers, and operational amplifiers.

Introduction

Operation of regular bulk MOS devices is usually limited to approximately 200°C because of the increase of the junction leakage current. Other device parameter variations, such as the reduction of mobility and the shift of threshold voltage with temperature, are limiting factors as well. SOI MOSFETs present very small junction areas, and their high-temperature leakage currents can be 3 to 4 orders of magnitude lower than those of regular MOS devices [1]. In addition, the threshold voltage variation with temperature is much smaller in SOI than in bulk. In this paper, we analyze the evolution of these and other important parameters in SOI transistors and circuits with temperature. The cases of both fully-depleted SOI and Gate-All-Around (GAA) [2] technologies are considered (Fig. 1).

Device Fabrication

All SOI devices were fabricated using commercially available SIMOX material. The silicon overlayer was thinned down in order to obtain a final silicon thickness of 100 nm in the conventional SOI MOSFETs and 80 nm in the GAA devices. Lateral isolation was achieved using LOCOS for the SOI devices, while a mesa process was used for the GAA transistors. A 50 nm-thick gate oxide was grown and boron ion implantation was used to adjust the threshold voltage. After threshold implant, N^+ polysilicon was deposited and patterned to form the gate electrodes. Standard source and drain and back-end processes were performed to complete the fabrication. An aluminum/silicon alloy was used for the metallization. No special care was taken in order to optimize the process for high-temperature operation. The n-channel transistors are fully-depleted, enhancement-type devices, while the p-channel ones are accumulation-mode (deep-depletion) devices [3]. Temperature performances of the devices were measured by probing the wafers placed on a heated chuck. The upper temperature limit of this experimental set-up was 320°C.

Device parameters

Some device parameters, such as channel mobility, vary with temperature in SOI devices like in bulk MOSFETs. Some other parameters, on the other hand, vary in a different way. The device OFF current, equal to the junction leakage current in the case of enhancement-mode devices, is markedly smaller in SOI than in bulk transistors, owing to the reduced junction area (Fig. 2). This is also valid for accumulation-mode devices, *i.e.* with no junctions, because the leakage path is equivalently reduced, and I_{ON}/I_{OFF} ratios in excess of 10,000 and 100 are obtained at 200 and 300°C, respectively. Fig. 3 presents the leakage current in SOI and GAA devices as a function of temperature. It can be seen that the slope of the GAA curve is smaller than that in the SOI devices, owing to a better control of the potential in the silicon film by the surrounding gate electrode.

The threshold voltage of SOI fully-depleted transistors is known to be 2 to 3 times less sensitive on temperature than that of bulk devices. However, there exists a critical temperature (220°C in [4]) beyond which the device is no longer fully depleted, which causes the threshold voltage variation with temperature to be similar to that in a bulk device. In GAA devices, where depletion arises from both the top and the bottom of the silicon film, this critical temperature is increased substantially, such that minimal temperature dependence of the threshold on temperature is observed up to 320°C (Fig. 4).

The output conductance of transistors is an important parameter limiting the performances of analog CMOS ICs. It was observed that the output conductance of SOI MOSFETs actually improves when temperature is increased (Fig. 5). This can be explained by several mechanisms: impact ionization is reduced at the drain, excess minority carrier concentra-

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tion in the device body is reduced through increased recombination, and the source junction bias is reduced owing to an increased saturation current. As a consequence, avalanche, parasitic bipolar and kink effects [1] are all reduced.

Digital circuits

High-temperature behavior of SOI and GAA CMOS circuits was studied on basis of various prototypes, ranging from simple inverters and logic gates to frequency dividers. None of the circuit designs was optimized for high-temperature operation. Nevertheless, the major causes of failure in bulk CMOS logic at high temperature, *i.e.* excess power consumption and degradation of logic levels and noise margin, are observed to be much reduced in SOI and GAA. Latch-up is of course totally suppressed.

CMOS inverters in both technologies exhibit full functionality and very little change in static characteristics at temperatures up to 320°C. Fig. 6 shows the results for GAA devices. The switching voltage remains stable, owing to the remarkably weak and symmetrical variation of the n and p threshold voltages (Fig. 4). The output voltage range is reduced from only a few millivolts, due to the slightly increased leakage current of the OFF device and the reduced carrier mobility of the ON device.

In logic gates with series transistors, such as AND and NAND gates, the increase of standby supply current with temperature remains even more limited than expected on basis of the leakage current of all constituent devices (Fig. 7). This is because in SOI circuits, the drain leakage current of each individual transistor flows towards its source, and thus into the following transistor, unlike bulk circuits, where all drain leakage currents are collected by the substrate.

Circuit speed was tested on toggle-chain frequency dividers. Bulk dividers-by-32 implemented in static C^2MOS logic style started to behave erratically around 180°C and became totally disfunctional at about 225°C. Similar implementations in SOI technology were still functional up to 320°C at a maximum input frequency of 100 MHz (Fig. 8), which is about half the speed achieved at room temperature [5].

Dynamic characteristics were also investigated on a clocked NOR gate, followed by an inverter (Fig. 9). The gate capacitance of the inverter is first precharged, which gives a low output voltage. Then, the capacitance is allowed to discharge or not, depending on the input values of the gate. But even when all nMOS input transistors are OFF, the internal node is discharged by leakage currents, yielding a limited holding time. At room temperature, this parasitic discharge lasts about 20 µs and is slightly longer in GAA, owing to the higher gate capacitance of the inverter. At 320°C, the holding time, and thus the minimum operation frequency, are only reduced by a factor of 10 in both technologies. The slope of the output curves is limited by the slow discharge of the internal node at 25°C, and by the reduced drive capability of the output inverter (loaded by the 15 pF capacitance of an oscilloscope) at 320°C. It can be noted that the GAA inverter is faster, owing to the higher transconductance offered by the double gate structure.

Analog circuits

The performances of a folded cascode OTA (Operational Transconductance Amplifier) were studied (Fig. 10). The DC voltage gain A_{VO} of this amplifier is equal to the product of the gate transconductance of the input transistors and the global output impedance of the circuit [6]. The transition frequency f_T is only proportional to the gate transconductance of the input transistors. The use of twin-gate devices [7] with higher output impedance allows to increase the DC gain (Fig. 11).

The behavior at high temperature is consistent with what can be expected from the individual device characteristics. As the gate transconductance decreases and the output impedance increases, the transition frequency decreases but the DC gain of the amplifier remains quite stable (Fig. 12).

Finally, it is worth noting that the offset voltage remains between 0 and 2 millivolts for all temperatures.

Conclusions

This paper establishes the usefulness of SOI and GAA devices for high-temperature applications. Enhancement-mode and accumulation-mode fully-depleted transistors in both technologies show high-temperature performances which are far superior to those of bulk MOSFETs. Satisfactory operation of both analog and static and dynamic digital circuits has been demonstrated up to 300°C.

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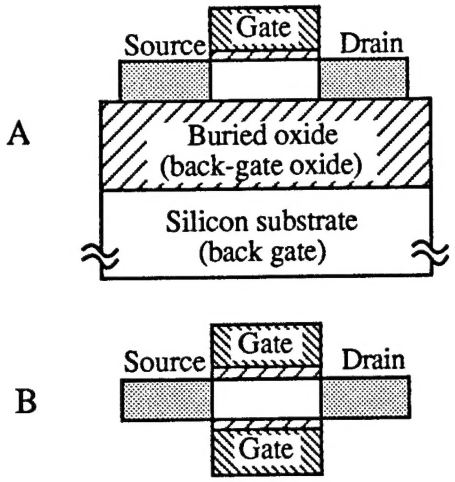

Fig. 1: Conventional thin-film SOI MOSFET (A) and GAA MOSFET (B).

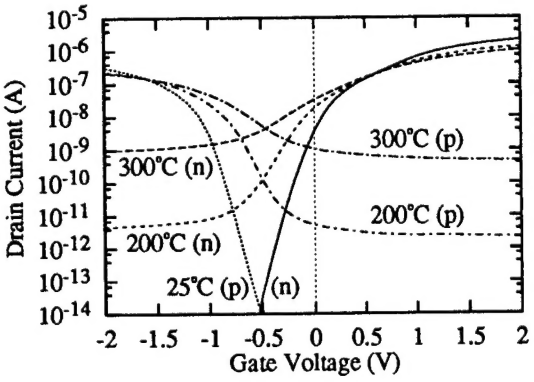

Fig. 2: Log $I_d(V_g)$ of n- and p-channel SOI MOSFETs at different temperatures. W/L=3μm/3μm, V_{ds}=±50 mV.

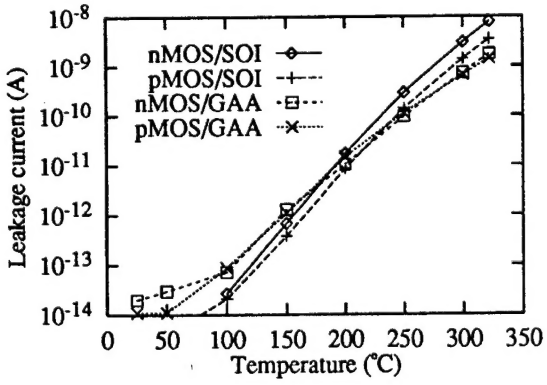

Fig. 3: Leakage current in regular SOI and GAA transistors as a function of temperature. W/L=3μm/3μm, V_{gs}=±1.5V, V_{ds}=±1V.

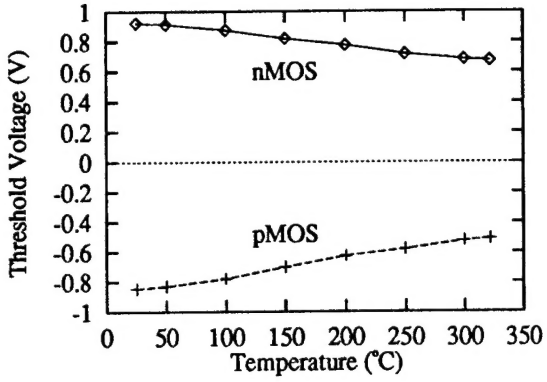

Fig. 4: Threshold voltage in GAA devices as a function of temperature.

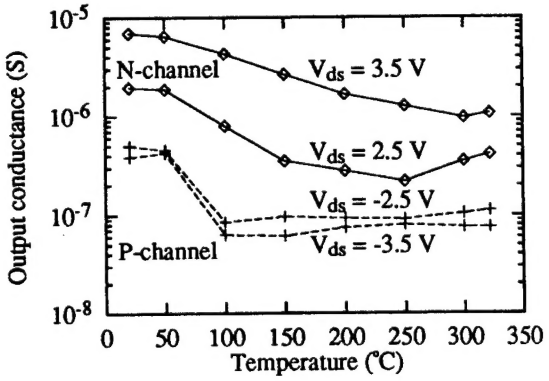

Fig. 5: Output conductance of SOI transistors as a function of temperature. W/L=50μm/10μm, V_{gs}=±1.5V.

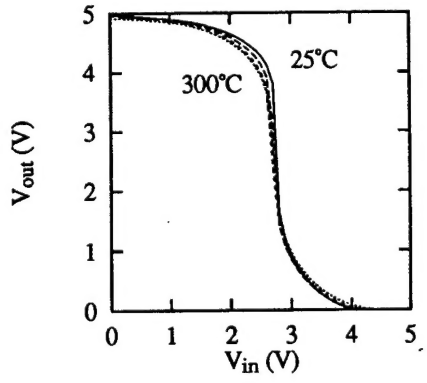

Fig. 6: Transfer characteristics of a GAA inverter at 25, 100, 200 and 300°C.

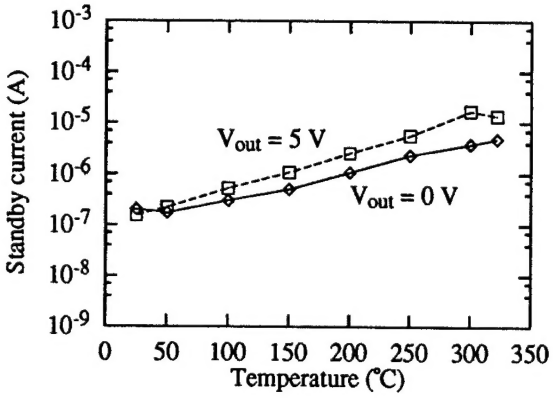

Fig. 7: Static power consumption of a SOI/CMOS AND gate with 5V power supply.

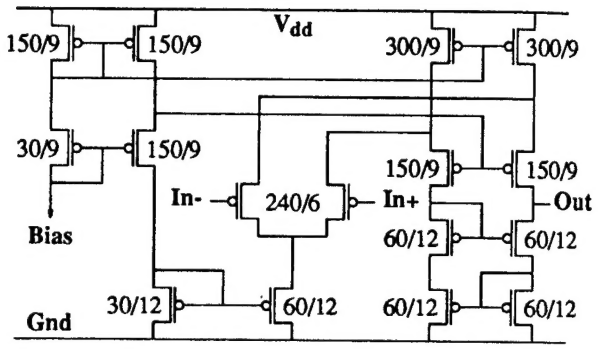

Fig. 10: Diagram of the operational amplifier with regular SOI transistors. The W/L's of the transistors are presented.

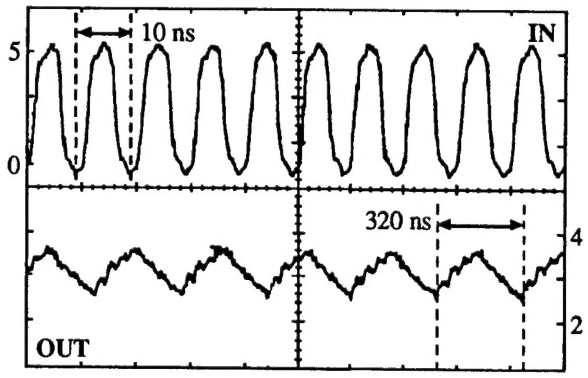

Fig. 8: Measured input (100 MHz) and output (3.125 MHz) signals of a SOI/CMOS divide-by-32 circuit operating at 300°C.

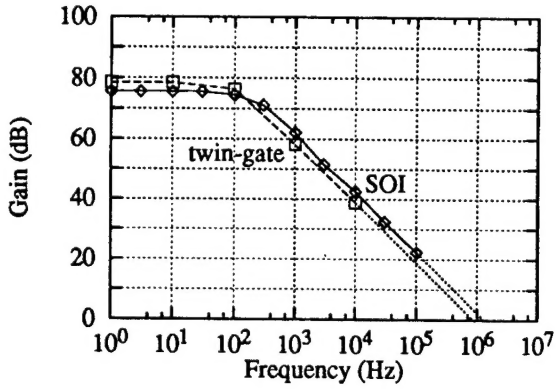

Fig. 11: Bode diagram of regular and twin-gate fully-depleted SOI operational amplifiers at 25°C.

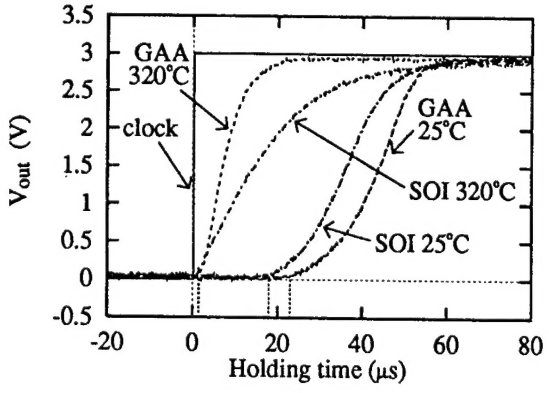

Fig. 9: Response of SOI and GAA dynamic OR gates at 25 and 320°C.

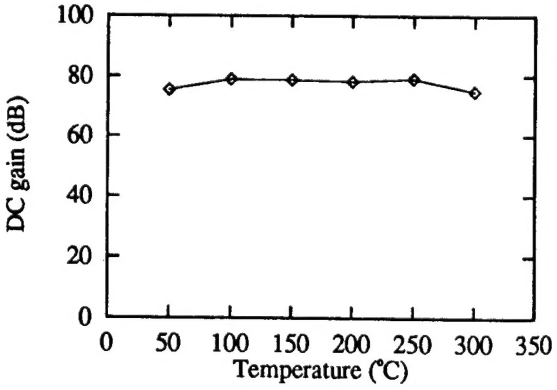

Fig. 12: DC gain of an SOI operational amplifier *vs.* temperature.